REMARKS

Claims 59-60, 62, 64, 66-84 and 92-94 are pending in this application.

At the outset, Applicant notes that notes that the limitations "a plurality of contact holes . . . having reduced sidewall striations" (claim 56) and "a plurality of recesses . . . having reduced striations" (claim 92) that result from "the application of a first power level plasma of an etching gas . . . for a first predetermined time followed by the application of a second power level plasma of said etching gas . . . for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma" are not product-by-process limitations, as the last Office Action asserts, but rather *resulting structures* having defined and distinct characteristics.

In R2 Medical Systems, Inc. v. Katecho, Inc., which involved a claim reciting that one element be "affixed" to another, the court found that "'affixed' means 'to be attached physically.'" R2 Medical Systems, Inc. v. Katecho, Inc., 931 F.Supp. 1397, 1425-26 (N.D. Ill. 1996). The Court held that "[t]he terms of the claims do not indicate that 'affixed' refers to a process by which the stannous chloride is bound to the conductive plate, but only that it refers to the result of that process." Id. (quoting CVI/Beta Ventures, Inc. v. Custom Optical Frames, Inc., 893 F. Supp. 508, 519 (D. Md. 1995) (limitation that element be in 'work-hardened pseudoelastic metallurgic state' is directed to the structure, not the process, of manufacture)).

In Hazani v. U.S. Int'l Trade Comm'n, which involved patent claims to a memory cell comprising a conductive plate having a surface that was "chemically engraved," the Federal Circuit also held that the claims were "pure product claims" and not product-by-process claims. Hazani v. U.S. Int'l Trade Comm'n, 126 F.3d 1473, 44 USPQ2d 1358 (Fed. Cir. 1997). The Federal Circuit reasoned that the "chemically engraved" limitation, read in context, described the product more by its structure rather than by the process used to obtain it. Id.

In the present case, the above-noted limitations of independent claims 56 and 92 are structural limitations and not product-by-process limitations. Like the "chemically engraved" plate of Hazani, a plurality of "contact holes" or "recesses" having reduced sidewall striations "resulting from the application of a first power level plasma of an etching gas . . . for a first predetermined time followed by the application of a second power level plasma of said etching gas . . . for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma" are *resulting structures* having distinct and defined characteristics.

Claims 59-60, 68-84 and 92-94 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Irinoda, U.S. Patent No. 5,726,499 ("Irinoda"). This rejection is respectfully traversed.

The claimed invention relates to an integrated circuit structure with specific structural features obtained by a particular process methodology. As such, independent claim 59 recites an "integrated circuit substrate" comprising *inter alia* "a substrate," "an oxide layer formed over said substrate," and "a plurality of cylindrical contact holes formed in said oxide layer, said plurality of contact holes extending to a topmost surface of said oxide layer and having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes." Independent claim 59 also recite that the reduced sidewall striations result "from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma."

Independent claim 92 recites an integrated circuit substrate comprising *inter alia* a substrate, an oxide layer formed over the substrate and "a plurality of recesses formed in said oxide layer, sidewalls of said recesses forming sidewalls of cylindrical contact holes extending to a topmost surface of said oxide layer and having reduced striations." Independent claim 92 also recites that the plurality of cylindrical contact holes formed in

said oxide layer having reduced sidewall striations result "from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma." Independent claim 92 further recites that the "substrate has a decreased critical dimension (CD) loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma."

Irinoda relates to a contact structure having a ring-shaped wall member formed in a depression of an insulation layer. (Abstract). Specifically, in FIGS. 5A-5E, Irinoda discloses a method of forming a contact hole 102A having a polysilicon ring 105A positioned above the contact hole 102A, such that the diameter of the contact hole is substantially identical to the inner diameter of the ring 105A. (Col. 11, lines 34-35). The method disclosed by Irinoda includes etching a substrate having "an insulation layer 102" and a "silicon nitride layer 104" to form a depression 103. (Col. 10, line 37 to col. 11, line 1). A polysilicon layer 105 is deposited on the surface of the silicon nitride layer 104 and within the depression 103. (Col. 11, lines 5-6). An anisotropic etching process is applied to the polysilicon layer. (Col. 11, lines 10-11). The etching stops when the surface of the silicon nitride layer 104 and the bottom of the depression 103 are both exposed. (Col. 11, lines 17-19). The etching step results in the formation of a polysilicon ring 105A, which acts as an etching mask for creating a contact hole 102A. (Col. 11, lines 32-34).

Irinoda does not disclose all limitations of claims 59-60, 68-84, 92 and 93. Irinoda fails to disclose, teach or suggest an integrated circuit substrate having "a plurality of cylindrical contact holes . . . having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes," as independent claim 59 recites. Irinoda is also silent about "a plurality of recesses . . . having reduced striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of

said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma, and wherein said substrate has a decreased critical dimension (CD) loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma," as independent claim 92 recites.

Irinoda is silent about a first and second power level plasma, much less about "a plurality of recesses" with "reduced striations resulting from the application of a first power level plasma of an etching gas . . . for a first predetermined time followed by the application of a second power level plasma of said etching gas . . . for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma, and wherein said substrate has a decreased critical dimension (CD) loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma," as independent claim 92 recites. For at least these reasons, Irinoda fails to disclose all limitations of claims 59-60, 68-84 and 92-94, and withdrawal of the rejection is respectfully requested.

Claims 62, 64 and 67 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Irinoda in view of Summerfelt et al., U.S. Patent No. 5,612,574 ("Summerfelt"). The rejection is respectfully traversed.

Claims 62, 64, and 67 relate to the integrated circuit substrate of independent claim 59, and recite that the substrate is germanium, gallium arsenide, or a DRAM substrate, respectively.

Summerfelt relates to a semiconductor structure "using high-dielectric-constant materials and an adhesion layer." (Abstract; Title). Summerfelt teaches that "an interlevel isolation layer" and a "barrier layer" are formed over the active region and "disposed outwardly from the conductive plug." (Col. 2, lines 42-46). "[A]n oxygen-stable inner electrode is formed outwardly from portions of the interlevel isolation layer and the barrier layer." (Col. 2, lines 46-48). Summerfelt also teaches that "[A]n adhesion layer is disposed between the oxygen-stable inner electrode and the interlevel isolation layer and

the barrier layer." (Col. 2, lines 48-51). In this manner, "the problems of adhesion between the oxygen-stable layer and the interlayer isolation layer in devices including such materials" are eliminated. (Col. 2, lines 29-32).

Irinoda and Summerfelt, whether considered alone or in combination, fail to teach or suggest all limitations of independent claim 59. As discussed above with respect to claims 59-60, 68-84 and 92-94, Irinoda fails to teach each and every limitation of independent claim 59. In addition, Summerfelt is silent about "a plurality of cylindrical contact holes" formed in an oxide layer, much less about "a plurality of cylindrical contact holes" formed in an oxide layer and "having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes," as independent claim 59 recites. For at least these reasons, Irinoda and Summerfelt, whether considered alone or in combination, fail to disclose, teach or suggest all limitations of independent claim 59, and withdrawal of the rejection of claims 62, 64 and 67 is also respectfully requested.

Claim 66 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Irinoda in view of Foote el al., U.S. Patent No. 5,710,067 ("Foote"). This rejection is respectfully traversed.

Foote relates to a silicon oxime film formed by plasma enhanced chemical vapor deposition. (Abstract). The silicon oxime film is useful as an anti-refection layer during photolithography, as an etch stop, and as a protection layer. (Abstract).

Irinoda and Foote, whether considered alone or in combination, fail to teach or suggest all limitations of independent claim 59. As discussed above, Irinoda fails to teach each and every limitation of independent claim 59. In addition, Foote teaches only an antireflective coating formed over a substrate, and not the limitations of independent claim 59. For at least these reasons, Applicant submits that claim 66 is also allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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